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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/593,765	06/14/2000	Hisashi Ohtani	0756-2149	8038

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EXAMINER
NGUYEN, CUONG QUANG

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N . 09/593,765	Applicant(s) OHTANI ET AL.	
	Examiner Cuong Q Nguyen	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-52 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-52 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The amended title "SEMICONDUCTOR DEVICE" is not descriptive. A more specific title is required.

Claim Rejections - 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 4, 6- 9, 11, 13-16, 18, 20-24, 26, 28-30, 48, 49, 51, are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang et al. (US 5,424,244).

Zhang et al. discloses a semiconductor device comprising: a semiconductor layer (204, a crystal silicon layer) formed on a surface of an insulating layer (203), the semiconductor including a first impurity region (208), a second impurity region (209), and a channel region in therebetween; a gate insulating film (205) formed on the semiconductor layer; a gate electrode (206) formed on the gate insulating film; a first insulating film (207) formed over the insulating surface, semiconductor layer, gate insulating film and gate electrode; a second insulating film (210, a polyimide organic resin layer) formed on the first insulating film; an electrode (213) formed on the second

insulating film and connected to the second impurity region (209); a transparent pixel electrode (211, an ITO layer) formed on the second insulating film, wherein the pixel electrode electrically connected to the electrode and is located under the electrode. See Zhang et al.'s Fig.11.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-11, 13-18, 20-26, 28-30, 48- 51, are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Hsieh (US 5,153,142) in view of Tran et al. (US 5,273,910).

Hsieh discloses a semiconductor device comprising: a doped polysilicon layer (14) formed on a surface of an insulating layer (12), the polysilicon layer including source/drain regions, and a channel region in therebetween; a gate insulating film (16) formed on the poly silicon layer; a gate electrode (18) formed on the gate insulating film; a first insulating film (20, a silicon oxide layer) formed over the insulating surface, semiconductor layer, gate insulating film and gate electrode; an electrode (32, an

aluminum layer) formed over the second insulating film and connected to one of source/drain regions; a transparent pixel electrode (30, an ITO layer) formed over the second insulating film, wherein the pixel electrode electrically connected to the electrode and is located under the electrode. See Hsieh's Fig.8.

Hsieh does not teach that the layer (14) is a single crystal silicon layer which includes a first impurity region, a second impurity region, and a channel region in therebetween; a second insulating film of a polyimide organic resin layer formed between the electrode, pixel electrode and the first insulating film.

Tran discloses a semiconductor device comprising: a semiconductor layer (42) can be formed of a single crystal silicon or a polysilicon layer on a surface of an insulating layer (51), the semiconductor including a first impurity region (45), a second impurity region (46), and a channel region in therebetween; a gate insulating film (43) formed on the semiconductor layer; a gate electrode (49) formed on the gate insulating film; a first insulating film (a planarization layer 53) formed over the insulating surface, semiconductor layer, gate insulating film and gate electrode; the planarization layer is planarized by coating with a second insulating film (a coating layer of polyimide organic resin layer) formed on the first insulating film to planarize the first insulating film (53). See Tran's Fig.5b and col.10 lines 8-32 and col.9 lines 60-64.

It would have been obvious to one of ordinary skill in the art to form the layer (14) in Hsieh's device of a single crystal silicon layer instead of polysilicon layer as taught

by Tran et al. because single crystal silicon and polysilicon are common materials for forming the channel region in the thin film transistor device and they are interchangeable. It also would have been obvious to one of ordinary skill in the art to coat the first insulating film (20) in Hsieh's device with a polyimide layer as taught by Tran in order to obtain a smooth planarization layer (see Tran's col.10, lines 8-32). One of ordinary skill would have been motivated to do so because it is easier to form other element such as metalization on top of a smooth planarization interlayer insulating film than an uneven surface interlayer insulating film as shown in Hsieh's device.

Claims 5, 12, 19, 17, 31-47 and 52, are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Hsieh in view of Tran et al. and further in view of Liauh (US 5,027,185).

Hsieh and Tran teach all the limitations of claims 1-4, 6-11, 13-18, 20-26, 28-30, as shown above. However, Hsieh and Liauh do not teach that the conductor comprises a second conductive film of TiN.

Regarding claims 5, 12, 19, 27, 31-35, 52, Liauh discloses a semiconductor device having electrodes connected to source/drain regions (3) comprise a first conductive film (11, an Al layer) and a second conductive film (10, a TiN layer) between the first conductive film and source/drain regions. See Liauh's Fig.8.

It would have been obvious to one of ordinary skill in the art to form the electrode of double layer TiN/Al as taught by Liauh because TiN layer acts as a barrier layer to

prevent the migration of Al layer into the silicon source /drain regions which causes the junction spiking. See Liauh's col.2, lines 44-49.

Regarding claims 36-41, as above the electrode is formed of a TiN layer under an Al layer, therefore it is inherent that the TiN is interposed between the pixel electrode and the Al layer.

Regarding claims 42-47, as shown in Hsieh's Fig.8, another electrode formed the same material as the electrode connected to another source/drain region.

Response to Arguments

4. Applicant's arguments with respect to claims 1-47 have been considered but are not persuasive.

Applicants argue that the anodically oxidized layer (207) of Zhang et al. is not the same as the first insulating film of the present invention such as it is not formed over the insulating surface, the semiconductor layer, the gate insulating film, and the gate electrode. In response, as shown in Zhang et al.'s Fig.11(E), the anodically oxidized layer (207) is clearly formed over the gate electrode (206), over the gate insulating film (205), and over the surface of insulating layer (203) and the semiconductor layer (204) under the gate electrode.

Applicants argue that neither Hsieh nor Tran et al. teaches the second insulating film comprising an organic resin formed on the first insulating film. In response, as above discussed, Tran et al. clearly teaches the second insulating film of polyimide

organic resin coating the first insulating (53) to planarize the first insulating film (Tran et al.'s col.10, lines 8-32). So, it would have been obvious to one of ordinary skill in the art to incorporates the organic resin coating as taught by Hsieh into Hsieh's device in order to obtain a smooth planarization first insulating film.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the n tice published in th Official Gaz tt , 1096 OG 30 (Nov mb r 15, 1989). Th Group 2811 Fax Cent r numb r is (703) 308-7722

and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

7. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Tom Thomas

CN

January 16, 2002

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800